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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/628,900	ZARRIEFF ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *011005, 072803*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: IDSs dated 1/10/05 and 7/28/03.

2. Claims 1-53 are presented for examination.

Claim Objections

3. Claims 2-11, 13-20, 22-27 are objected to because of the following informalities:

a. Regarding claims 2-11, on the first line of each claim "A control system" should be changed to "The control system", for purposes of clarity.

b. Regarding claims 13-20 and 51-53, on the first line of each claim, "A data transfer circuit" should be changed to "The data transfer circuit", for purposes of clarity.

c. Regarding claim 22-27, on the first line of each claim, "A control system" should be changed to "The control system", for purposes of clarity.

d. Regarding claims 29-35 and 37-42, on the first line of each claim, "A method" should be changed to "The method", for purposes of clarity.

e. Regarding claim 44-49 on the first line of each claim, "One or more computer-readable media" should be changed to "The computer readable media", for purposes of clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 4, 5, 11, 12, 14-16, 19, 20, 28, 29, 31-33, 50, 51 and 53 are rejected under 35 U.S.C. 102(b) as being anticipated by Koostra et al., U.S. Patent 5,416,434.

6. Regarding claim 1, Koostra teaches a control system comprising:

a. a data circuit (processor, col. 4, lines 42-49) configured to communicate computer readable data with a component (memory, col. 4, lines 42-49) via a data transfer bus (not disclosed but a data transfer bus is inherent in order for a processor to access a memory component);

b. a control circuit configured to control a frequency spread deviation for data communication via the data transfer bus (Shift Register 102, MUX 104, and J-K flip-flop 108, figure 3);

c. a data register (inherent in function block 16 within SELECT 116 in order to receive ACCESS input 20, INTERRUPT input 22 and MODE input 24, col. 3, lines 21-54 and figures 1 and 3) configured to maintain an operating conditions status of the data circuit (wherein the operating conditions are interpreted to be an access, interrupt or a mode of the processor, col. 3, lines 21-54 and figure 1), the operating conditions status corresponding to data communications loading on the data transfer bus (an access, col. 3, lines 28-37, lines 45-66 and figure 1);

d. control logic configured to:

i. obtain the operating conditions status from the data register (registers inherently within SELECT circuit 116, figure 3); and

ii. generate a control circuit input to adjust the frequency spread deviation according to the operating conditions status (output of SELECT 116).

7. Regarding claim 4, Koostra taught the control system according to claim 1, as described above. Koostra further teaches wherein the control circuit is further configured to control the frequency spread deviation by adjusting a minimum clock frequency and a maximum clock frequency for data communication (higher and lower frequencies, col. 1, lines 35-47).

8. Regarding claim 5, Koostra taught the control system according to claim 1, as described above. Koostra further teaches wherein the control circuit is configured to control the frequency spread deviation by adjusting a percentage clock frequency deviation from a center frequency for data communication (dithering, col. 1, line 67 through col. 2, line 5; dithering inherently adjusts a percentage clock frequency deviation from a center frequency).

9. Regarding claim 11, Koostra taught the control system according to claim 1, as described above. Koostra further teaches wherein the control logic is further configured to generate the control circuit input to adjust the frequency spread deviation to minimize electromagnetic emissions associated with data communication via the data transfer bus (decreasing the magnitude of radiated emissions, col. 1, lines 43-47).

10. Regarding claim 12, Koostra teaches data transfer circuit (circuit in figure 1) configured to adjust a frequency spread deviation for spread spectrum clocking of a data transfer via a data transfer bus according to operating conditions (wherein the operating conditions are interpreted to be an access, interrupt or a mode of the processor, col. 3, lines 21-54 and figure 1) of the data

transfer circuit, the operating conditions corresponding to data transfer bus loading (wherein the data transfer bus loading is based on the accessing/mode/interrupt, col. 1, lines 35-47).

11. Regarding claim 14, claim 14 is rejected for the same reasons as set forth in the rejection of claim 4.

12. Regarding claim 15, claim 15 is rejected for the same reasons as set forth in the rejection of claim 5.

13. Regarding claim 16, it is rejected for the same reasons as set forth hereinabove in the rejections of claim 1.

14. Regarding claims 19 and 20, they are rejected for the same reasons set forth hereinabove as in claims 11 and 12.

15. Regarding claims 28, 29, 31-34, 50, 51 and 53, Koostra taught claimed control system therefore he also teaches the claimed method and the claimed data transfer system.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claim 2 is rejected under 35 U.S.C. 102(b) as anticipated by Koostra, or, in the alternative, under 35 U.S.C. 103(a) as obvious over Koostra in view of Swanson, U.S. Patent 6,670,834.

18. Regarding claim 2, Koostra taught the control system according to claim 1, as described above. Koostra further appears to teach wherein in the control circuit is a phase-locked loop (Shift Register 102, MUX 104, and J-K flip-flop 108, figure 3) configured to receive the control circuit input and adjust the frequency spread deviation. In Koostra Shift Register 102 together with MUX 104, and J-K flip-flop 108 in figure 3 appears to act as a phase-locked loop. Specifically, the circuit has a phase detector implemented by J-K flip-flop 108 and has feedback to its input via shift register 102 and MUX 108. Thus, the control circuit of Koostra functions as a phase-locked loop.

Even if Koostra does not teach wherein the control circuit is a phase-locked loop, Swanson teaches a phase-locked loop (figure 1) that is used to produce a dithered clock output. Swanson provides the advantage of having a phase lock loop that operates reliably and checks to ensure that the system is actually dithering as expected.

It would have been to one of ordinary skill in the art, having the teachings of Koostra and Swanson before them at the time the invention was made, to modify the control circuit to implement the phase-locked loop of Swanson.

One of ordinary skill in the art would have motivated to make this modification in order to provide the advantage of ensuring that the system is actually dithering as expected in view of the teachings Swanson. This advantage would be desirable in Koostra.

19. Claims 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Swanson, U.S. Patent 6,670,834.

20. Regarding claim 17, Koostra taught the data transfer circuit according to claim 12, as described above. Koostra teaches wherein the data transfer circuit is further configured to obtain an operating condition status from a data register (registers inherently within SELECT circuit 116, figure 3). However, Koostra does not explicitly disclose wherein the operating conditions status corresponds to process, voltage and temperature operating conditions of the data transfer circuit.

Swanson teaches wherein the operating conditions status corresponds to process, voltage and temperature operating conditions of the data transfer circuit (col. 5, lines 25-30). Swanson provides the advantage of having a phase lock loop that operates reliably and checks to ensure that the system is actually dithering as expected.

It would have been to one of ordinary skill in the art, having the teachings of Koostra and Swanson before them at the time the invention was made, to modify the data register of Koostra to include operating condition corresponding to process, voltage and temperature operating conditions of the data transfer circuit as taught by Swanson.

One of ordinary skill in the art would have motivated to make this modification in order to provide the advantage of ensuring that the system is actually dithering as expected in view of the teachings Swanson. This advantage would be desirable in Koostra.

21. Claims 3, 13 and 35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Refaeli et al., U.S. Patent Application Publication 2004/00762221.

22. Regarding claim 3, Koostra taught the control system according to claim 1, as described above. Koostra does not explicitly disclose wherein operating conditions of the data circuit include at least one of a process, a voltage, and a temperature operating condition.

Refaeli teaches wherein operating conditions of a data circuit include at least one of a process, a voltage and a temperature operating condition (the behavior of the spread spectrum clock generator can vary when the ***temperature*** of the device that it is coupled to varies, wherein the data circuit is the device, paragraph [0007] and paragraph [0016]). Refaeli further teaches that an advantage of compensating for variations in the temperature of the device is achieved (paragraph [0005] and paragraph [0007]).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Refaeli before them at the time the invention was made to modify the control system of Koostra to include adjusting the frequency spread deviation according to at least one of a process, a voltage and a temperature of the data circuit as taught by Refaeli.

One of ordinary skill in the art would have been motivated to make this modification in order to achieve the advantage of compensating for the variations in the temperature of the device that affect a spread spectrum clock. This advantage would be desirable in Koostra.

23. Regarding claims 13 and 35, it is rejected for the same reasons as set forth hereinabove in the rejection of claim 3.

24. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Tanenbaum, "Structured Computer Organization".

25. Regarding claim 10, Koostra taught the control system according to claim 1, as described above. Koostra does not explicitly disclose wherein control logic is implemented as firmware in the control system. The control logic of Koostra appears to be implemented as hardware.

Tanenbaum teaches hardware and software are logically equivalent and that any instruction executed by the hardware can also be implemented in software (page 11). Further Tanenbaum teaches that firmware is software that is embedded in electronic devices that may be changed. Tanenbaum teaches that software provides the advantage of being easily changeable (page 11).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Tanenbaum before them at the time of the invention, to modify the control logic to be implemented as firmware in the control system.

One of ordinary skill in the art would have been motivated to make this modification in order to make the system more easily changeable in view of the teachings of Tanenbaum.

26. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Newton, "Newton's Telecom Dictionary"

27. Regarding claim 6, Koostra taught the control system according to claim 1, as described above. Koostra does not explicitly disclose the further comprising an application specific integrated circuit (ASIC) that includes the data circuit, the control circuit, and the data register.

Newton teaches that an ASIC is used to consolidate many chips into a single package thereby providing the advantage of reducing system board size and reducing power consumption (definition of ASIC, page 63).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Newton before them at the time the invention was made, to modify the circuitry of Koostra to include the data circuit, the control circuit and the data register of Koostra in an application specific integrated circuit in as taught by Newton.

One of ordinary skill in the art would have been motivated to make the modification in order to achieve the advantages of reducing system board size and reducing power consumption in view of the teachings of Newton. These advantages would be desirable in Koostra.

28. Regarding claim 7, Koostra together with Newton taught the control system according to claim 6, as described above. Koostra further teaches wherein:

a. the component is a memory component (memory, col. 4, lines 42-49);

b. the data transfer bus is a memory bus (not disclosed but a data transfer bus is inherent in order for a processor to access a memory component);

c. the data circuit is further configured to communicate the computer readable data to the memory component via the memory bus (processor accessing memory, col. 4, lines 42-49);

29. Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra and Newton, "Newton's Telecom Dictionary" in further view of To et al., U.S. Patent 6,631,338 and Swanson, U.S. Patent 6,670,834.

30. Regarding claim 8, Koostra together with Newton taught the control system according to claim 6, as described above. Koostra and Newton do not explicitly disclose wherein the ASIC further includes variable connection drive pads, and wherein operating conditions include,

process, voltage and temperature conditions. However, it is inherent that an ASIC would have connection drive pads.

To teaches variable connection drive pads (FETs set the drive strength at pad 10, col. 2, lines 26-49). To further teaches the variable connection drive pads provide the advantage of compensating for on die process variation.

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra, Newton and To before them at the time the invention was made, to modify the connection drive pads of the combination of Koostra and Newton to include the variable connection drive pads as taught by To.

One of ordinary skill in the art would have been motivated to make this modification in order to compensate for the on die process variation in view of the teachings of To.

Swanson teaches wherein operating conditions include process, voltage and temperature conditions (col. 5, lines 26-30). The invention of Swanson is directed toward changing the delay and dithering associated with a clock which is similar to that of Koostra. Changing the delay and dithering inherently change the frequency spread deviation. Swanson provides the advantage of having a phase lock loop that operates reliably and checks to ensure that the system is actually dithering as expected.

It would have been to one of ordinary skill in the art, having the teachings of Koostra and Swanson before them at the time the invention was made, to modify the data register of Koostra to include operating condition corresponding to process, voltage and temperature operating conditions of the data transfer circuit as taught by Swanson.

One of ordinary skill in the art would have motivated to make this modification in order to provide the advantage of ensuring that the system is actually dithering as expected in view of the teachings Swanson. This advantage would be desirable in Koostra.

31. Claims 9 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra and Newton, "Newton's Telecom Dictionary" in further view of Knee et al., U.S. Patent 5,337,254.

32. Regarding claim 9, Koostra together with Newton taught the control system according to claim 6, as described above. Koostra and Newton do not explicitly disclose wherein the ASIC further includes variable connection drive pads, and wherein operating conditions of the ASIC vary according to a drive current strength of a variable connection drive. However, it is inherent that an ASIC would have connection drive pads.

Knee teaches variable connection drive pads (pad coupled to a programmable I/O circuit, figures 1 and 3 and related text), and wherein operating conditions of the ASIC vary according to a drive current strength of a variable connection drive pad (the drive strength changes according to measured process, voltage and temperature, col. 3, lines 18-35). Knee further teaches the variable connection drive pads provide the advantage of provide an adaptable output drive circuit for a chip which is responsive to both PVT parameter modifications and load capacitance changes. This advantage would be desirable in Koostra.

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra, Newton and Knee before them at the time the invention was made to modify the control of Koostra to include the variable connection drive pads as taught by Knee.

One of ordinary skill in the art would have been motivated to make this modification in order to provide the advantage of provide an adaptable output drive circuit for a chip which is responsive to both PVT parameter modifications and load capacitance changes.

33. Regarding claim 25, it is rejected for the same reasons as in the rejection of claim 9.

34. Claims 18 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in further view of Knee et al., U.S. Patent 5,337,254.

35. Regarding claim 18, Koostra taught the data transfer circuit according to claim 12, as described above. Koostra further teaches wherein the data transfer circuit is further configured to obtain an operating conditions status from a data register. Koostra does not explicitly disclose the operating conditions status varies according to a drive current strength of a variable connection drive pad.

Knee teaches variable connection drive pads (pad coupled to a programmable I/O circuit, figures 1 and 3 and related text), and wherein operating conditions vary according to a drive current strength of a variable connection drive pad (the drive strength changes according to measured process, voltage and temperature, col. 3, lines 18-35). Knee further teaches the variable connection drive pads provide the advantage of provide an adaptable output drive circuit for a chip which is responsive to both PVT parameter modifications and load capacitance changes. This advantage would be desirable in Koostra.

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Knee before them at the time the invention was made to modify the control of Koostra to include the variable connection drive pads as taught by Knee.

One of ordinary skill in the art would have been motivated to make this modification in order to provide the advantage of provide an adaptable output drive circuit for a chip which is responsive to both PVT parameter modifications and load capacitance changes.

36. Regarding claim 52, it is rejected for the same reason as in the rejection of claim 18.

37. Claims 21-24, 27, 36-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Newton, "Newton's Telecom Dictionary" and Swanson.

38. Regarding claim 21, Koostra teaches a control system comprising an integrated circuit and control logic wherein:

a. the integrated circuit (processor, col. 4, lines 42-49) is configured to transfer data to a memory component (memory, col. 4, lines 42-49) via a memory bus (not disclosed but a data transfer bus is inherent in order for a processor to access a memory component);

b. the integrated circuit including:

i. a clocking control configured to control a frequency spread deviation for data transfer via the memory bus (Shift Register 102, MUX 104, and J-K flip-flop 108, figure 3);

ii. a status register configured to maintain the status corresponding to memory bus loading (wherein the operating conditions are interpreted to be status such as an access, interrupt or a mode of the processor, col. 3, lines 21-54 and figure 1);

c. the control logic is configured to

i. obtain the status from the status register (wherein the status register is inherent in function block 16 within SELECT 116 in order to receive ACCESS input 20, INTERRUPT input 22 and MODE input 24, col. 3, lines 21-54 and figures 1 and 3; registers inherently within SELECT circuit 116, figure 3);

ii. generating a clocking control input to adjust the frequency spread deviation according to the status (output of SELECT 116).

Koostra does not explicitly disclose wherein the integrated circuit is an application specific integrated circuit (ASIC). Koostra also does not explicitly disclose wherein the status register is a process-voltage-temperature (PVT) status register to maintain the PVT status.

Newton teaches that an ASIC is used to consolidate many chips into a single package thereby providing the advantage of reducing system board size and reducing power consumption (definition of ASIC, page 63).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Newton before them at the time the invention was made, to modify the circuitry of Koostra to include the data circuit, the control circuit and the data register of Koostra in an application specific integrated circuit in as taught by Newton.

One of ordinary skill in the art would have been motivated to make the modification in order to achieve the advantages of reducing system board size and reducing power consumption in view of the teachings of Newton. These advantages would be desirable in Koostra.

Swanson teaches wherein operating conditions include process, voltage and temperature conditions (col. 5, lines 26-30). The invention of Swanson is directed toward changing the delay and dithering associated with a clock, which is similar to that of Koostra. Changing the delay

and dithering inherently change the frequency spread deviation. Swanson provides the advantage of having a phase lock loop that operates reliably and checks to ensure that the system is actually dithering as expected.

It would have been to one of ordinary skill in the art, having the teachings of Koostra and Swanson before them at the time the invention was made, to modify the data register of Koostra to include operating condition corresponding to process, voltage and temperature operating conditions of the data transfer circuit as taught by Swanson.

One of ordinary skill in the art would have motivated to make this modification in order to provide the advantage of ensuring that the system is actually dithering as expected in view of the teachings Swanson. This advantage would be desirable in Koostra.

39. Regarding claim 22, Koostra together with Newton and Swanson taught the control system according to claim 21, as described above. Koostra further appears to teach wherein in the control circuit is a phase-locked loop (Shift Register 102, MUX 104, and J-K flip-flop 108, figure 3) configured to receive the control circuit input and adjust the frequency spread deviation. In Koostra Shift Register 102 together with MUX 104, and J-K flip-flop 108 in figure 3 appears to act as a phase-locked loop. Specifically, the circuit has a phase detector implemented by J-K flip-flop 108 and has feedback to its input via shift register 102 and MUX 108. Thus, the control circuit of Koostra functions as a phase-locked loop.

Even if Koostra does not teach wherein the control circuit is a phase-locked loop, Swanson teaches a phase-locked loop (figure 1) that is used to produce a dithered clock output.

40. Regarding claim 23, Koostra together with Newton and Swanson taught the control system according to claim 21, as described above. Further regarding claim 23, it is rejected for the same reason as set forth in the rejection of claim 4 above.

41. Regarding claim 24, Koostra together with Newton and Swanson taught the control system according to claim 21, as described above. Further regarding claim 24, it is rejected for the same reason as set forth in the rejection of claim 5 above.

42. Regarding claim 27, it is rejected for the same reasons as set forth in the rejections of claim 11.

43. Regarding claims 36-42, Koostra together with Newton and Swanson taught the claimed control system therefore together they also teach the claimed method.

44. Claims 21-24, 27, 36-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra in view of Newton, "Newton's Telecom Dictionary", Swanson and Hardin, U.S. Patent 6,167,103 (cited in IDS dated 1/10/05).

45. Regarding claims 43-49, Koostra together with Newton and Swanson taught the claimed control system, as set forth hereinabove. Therefore together they also teach the one or more computer-readable media.

However, Koostra together with Newton and Swanson do not explicitly disclose wherein the control of a frequency spread deviation for data transfer is used in a printing device.

Hardin teaches control of a frequency spread deviation are used in computer or printing devices (wherein a spread spectrum clock in Hardin inherently controls the frequency spread

deviation, col. 1, lines 26-47; and wherein Hardin teaches that the frequency spread deviation is used in computers a printer, col. 2, lines 60-67).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra, Newton, Swanson and Hardin before them at the time the invention was made to modify Koostra, Newton, Swanson by implementing the claimed computer readable media to direct a printing device as claimed.

One of ordinary skill in the art would have been motivated to make the modification because a printing device would benefit from the advantages of reducing levels of radiated emissions in view of Koostra, reducing system board size and reducing power consumption in view of Newton and ensuring that the system is actually dithering as expected in view of the teachings Swanson.

46. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra together with Swanson in view of Tanenbaum, "Structured Computer Organization".

47. Regarding claim 26, Koostra together with Swanson taught the control system according to claim 21, as described above. Koostra and Swanson do not explicitly disclose wherein the control logic is implemented as firmware in the control system.

Tanenbaum teaches hardware and software are logically equivalent and that any instruction executed by the hardware can also be implemented in software (page 11). Further Tanenbaum teaches that firmware is software that is embedded in electronic devices that may be changed. Tanenbaum teaches that software provides the advantage of being easily changeable (page 11).

It would have been obvious to one of ordinary skill in the art, having the teachings of Koostra and Tanenbaum before them at the time of the invention, to modify the control logic to be implemented as firmware in the control system.

One of ordinary skill in the art would have been motivated to make this modification in order to make the system more easily changeable in view of the teachings of Tanenbaum.

48. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koostra and in further view of Knee et al., U.S. Patent 5,337,254.

49. Regarding claim 30, Koostra taught the method according to claim 28, as described above, further it is rejected for the same reasons set forth hereinabove in the rejection of claim 9.

Conclusion

50. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,774,687 to Gomm et al. teaches adjusting the delay in a phase lock loop based on the expected PVT environment.

U.S. Pat. No. 6,175,259 to Mann et al. teaches a programmable clock generator with two-tone modulation for EMI reduction.

U.S. Pat. No. 6,426,593 to Nieberger et al. teaches variable connection drive pad.

U.S. Pat. No. 6,980,581 to Sha et al. teaches an adaptive spread spectrum clock generator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James K. Trujillo
3/23/06

James K. Trujillo
Patent Examiner
Technology Center 2100